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Test power optimization with redundant transition test patterns in Digital Circuit

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Abstract: *In the design modelling of a DFT interface, the controlling and access operation defines the performance of BIST interfacing. In a DFT application, data stored in the BIST units are mapped to given query input and an output is developed as a match signal to which as decision is made. in the process of DFT operation, to obtain a faster matching and low power consumption, a new search approach and pattern alignment logic is defined. To improve the storage capacity of a DFT unit, a multi page interface is proposed. To the defined unit a new fault tolerance approach is integrated for a reliable, low power and fast processing DFTapplication.*

Keywords: *-DFT unit, low power, fast search, high volume, fault tolerant*

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I. Introduction

With the diversity in data accessing and emerging new technologies, new mode of data access is evolving. With this increment, the computation probability of data validation for data exchange or security concern is increasing. In a real time interface to govern data exchange router units are interfaced. Wherein to give a security monitoring firewalls, antivirus etc., are used. These applications operate on a permanently defined BIST content to which a input data is matched to obtain a validation of given data. this operation is performed with the support of a BIST unit. The DFT units are used as a database storage where a pre defined data are trained and on the requirement accessed to give a result. As the access probability are becoming dynamic with new technologies such as heterogonous network, cloud computing, distributed servers etc., the enhancement in performance reliability and efficiency of DFT interfacing is needed. To improve the performance of DFT interfacing, various developments were made in past. In [1], [2] using finite automata, or hashing approaches. A simple discrete comparator or a simple DFT having significant performance, whereas the area cost is very high [3], [4]. Evaluation of address matching with simple and regular expression will overcome the high area cost but significantly reduces the performance. One technique to increase the share of the cost of design principles and character comparisons and regular expressions and DFT-like approach [5], [6], [7], [8] is applied to reduce the search timing. The idea is to represent the characters are each represented by a single wire, resulting in a unique character. In this way, a character is reduced to a comparator whose input and gate count are reduced. In a binary decision diagram (BDD) presented in the form of a Boolean expression as multiple addresses representing tree-based structure of the DFT was outlined. In this way, the area cost is low compared to other DFT approach. More recently, fault tolerant has been proposed to address mapping various mixed techniques [9] suggested the use to the prefix mapping to read the rest of address and a record. [10] Presented an FPGA implementation of the bit-split string matching architecture. [11] Proposed to reduce the BIST size by relabeling states of AC state machine. Additionally, [12] proposed to use Label Transition Table and DFT-based Lookup Table to significantly reduce the BIST size. [13], [14] proposed a hash-based pattern matching co-processor where BIST is used to store the list of substrings and the state transitions. [15] Proposed a pattern matching algorithm which modifies the AC algorithm to consider multiple characters at a time. Furthermore, the content addressable memories (DFT) is also widely used for string matching because it can match the entire pattern at once when the pattern is shifted past the DFT. These developments were focused with the objective of faster mapping approach. however, with the emergence of new technologies and new devices, the constraint in resource demands for new solution. In this paper a new architecture with the objective of faster, low power, high volume and fault free condition is proposed. to outline the suggested approach this paper is defined in 6 sections. Wherein section 2 outlined the conational DFT interface architecture with the proposed architecture. Section 3 outlines the functional detail of the proposed architecture. Section 4 outlines the simulation results and section 5 concludes the presented approach.

II. DFT Interface Architecture

DFT unit are developed as an interface unit in accessing data from a pre allocated BIST location wherein the match of content, a data is retrieved. The conventional operation of DFT unit is illustrated in figure 1.

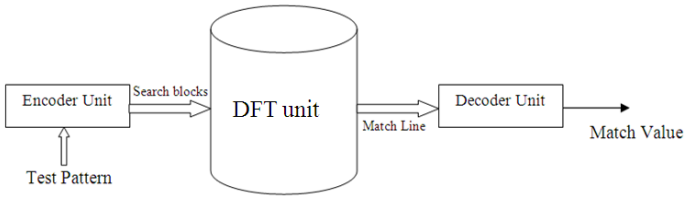


Figure 1: Interface unit for DFT unit

The conventional interface unit is observed to process the operation with a block generator unit, where the given pattern is transformed to a word block and passed to a comparator unit for match generation. The controller unit generate a FSM search operation of each search stage to make a decision. Wherein the DFT interface is observed to be operationally well designed, following constraint were observed with this design. The Redundant patterns in the BIST unit are making the DFT operation slower. The stored data at the BIST unit have High transition patterns consume a large power in storage and operation. In the storage of high volume data a linear BIST element for high volume storage is constraint in operation, and leads to slower operation. The storage error due to BIST fault and Fault conditions in BIST unit is resulting in wrong match output.

II. Functional Outline

The function operation of the proposed architecture operates in 3 working modes- Diagnosis, train and test mode. In the diagnosis mode, self-test operation is made. The BIST is filled with '0' and '1' to test stuck-0 or stuck-1 fault. Fault addresses are stored in Fault address_ register. In train mode patterns are buffered onto the BIST unit of DFT. The operation of the self test operation is illustrated in Figure 2.

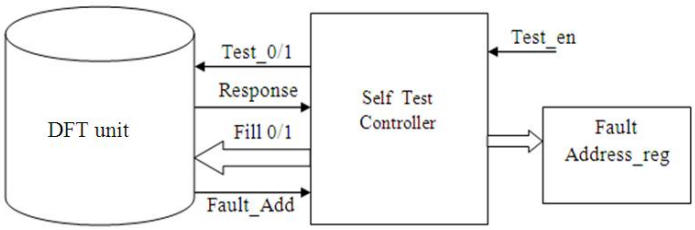


Figure 2: Fault testing operation in the DFT interface

The train signal is set high and patterns are given as input. Patterns are passed through aligner unit to give a shift alignment to reduce pattern transitions. Realigned patterns are buffered into addressed location. The address location is validated with fault address_ register to fill data. A redundancy of stored pattern is evaluated using hamming distance and new state transitions in controller unit is defined outlined in [15].On the test mode, a test pattern is given as input. The pattern is realigned and divided to blocks of 4 bit word. The word is passed to a comparator unit. The controller enables the reading of BIST content by enabling address_reg unit. The controller operates on a FSM mode where for the pattern testing a state flow using the conventional FSM flow and the proposed flow is illustrated in figure below. For a test pattern $abcd$ and $bbda$ the state transition is observed as,

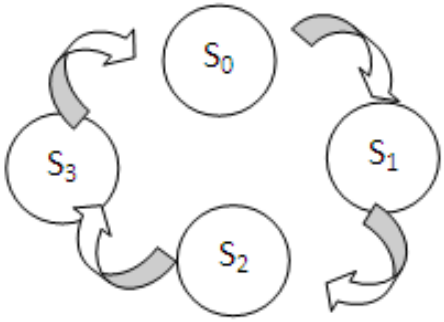


Figure 3: State transition flow in pattern matching using conventional approach

For a given pattern sequence is observed as,

$$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_0$$
$$a \rightarrow b \rightarrow c \rightarrow d$$

For the pattern $bbda$ again 4 state transitions are made,

$$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_0$$
$$b \rightarrow b \rightarrow d \rightarrow a$$

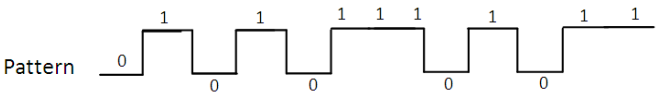
The total state transient observed is 8. Wherein it is observed that, a common pattern can move onto the same stage defined as,

$$a \rightarrow b \rightarrow c \rightarrow d$$
$$b \rightarrow b \rightarrow d \rightarrow a$$

This will result in a new state transition as,

Figure 4: The realigned pattern match in proposed system

The number of transition observed is minimized by 3 from 4 stages and a total stage is then observed to be 7.The new FSM controller is given in the controller unit and the pattern are passed on matching based on the selected state transition. To read the pattern, the address_reg generate a page address and location address to the address pointer. The address is validated from fault address_ register and BIST data is passed to the comparator A match signal is buffered and passed to match decoder. To conserve the power consumption in the DFT operation a aligner unit is proposed [15]. The aligner minimizes the transition pattern by linear shift operation illustrated in figure below



(a)

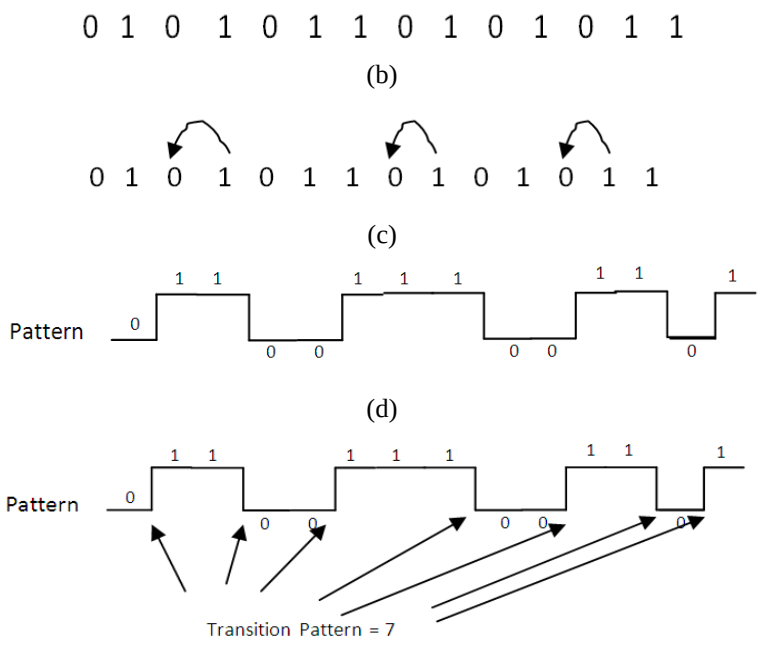


Figure 5: Reorder pattern in DFT operation (a) Original pattern, (b) Binary pattern, (c) Realignment operation, (d) Realigned Pattern, (e) Transition count

The power dissipation defined by,

$$P_d = \sum_{line} C_m V_{DD}^2 N_{tr}$$

Where N_{tr} are the number of tansiton observed, the total power is conserved based on the minimization of transiton. The aligned patterns are stored and used for matching with use less power in logical transitions.

IV. Simulation Results

To evaluate the performance of the proposed approach a timing result using a HDL definition for the encoder, decoder and BIST unit is developed based on VHDL coding, and simulated over Aldec's Active HDL for timing operational validation. To obtain the realization logic over a targeted PLD, Xilinx FPGA device of Virtex family is considered, and the implementation details gives the realization requirement for PLD implementation. The obtained observations are illustrated in below figures.

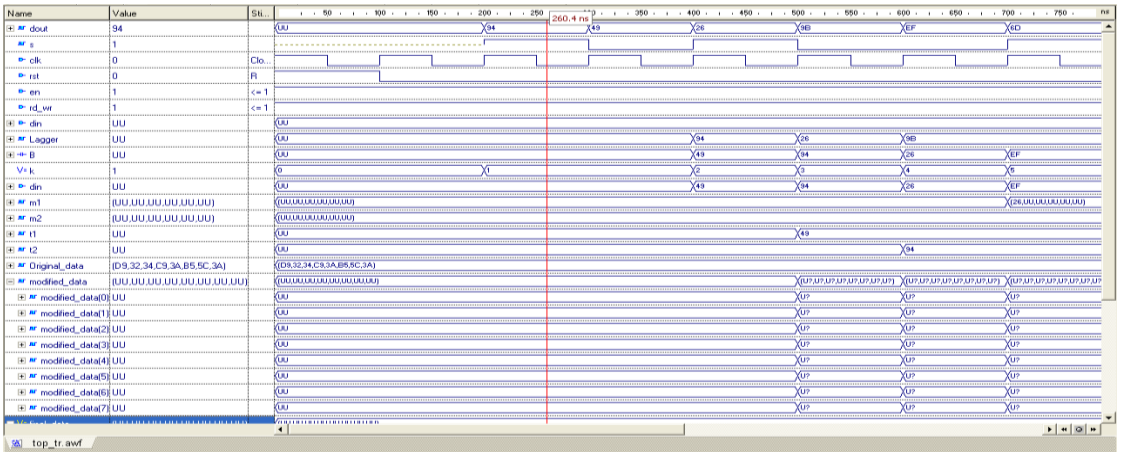


Figure 6. Simulation plot showing the observations made for the developed Sequencing algorithm

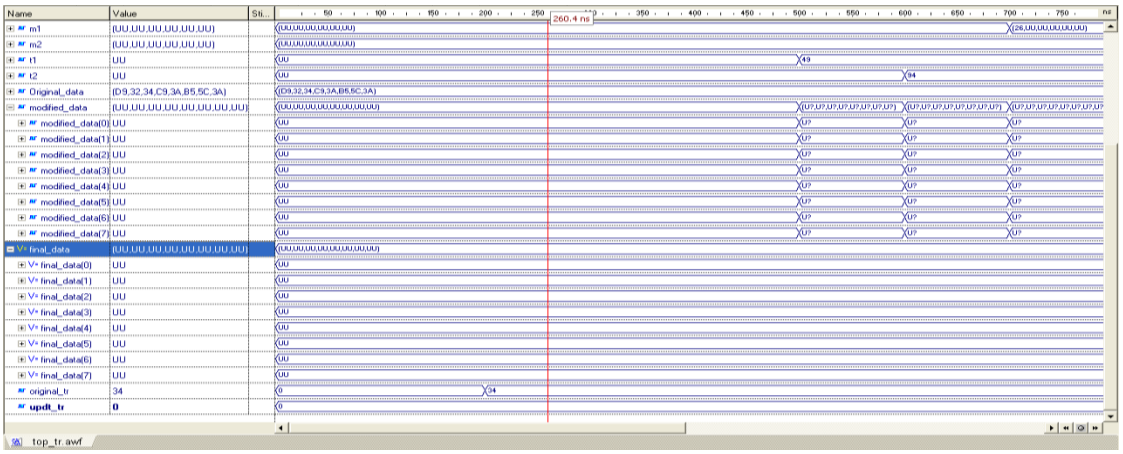


Figure 7. Figure illustrating the original data the modified data regenerated after coding

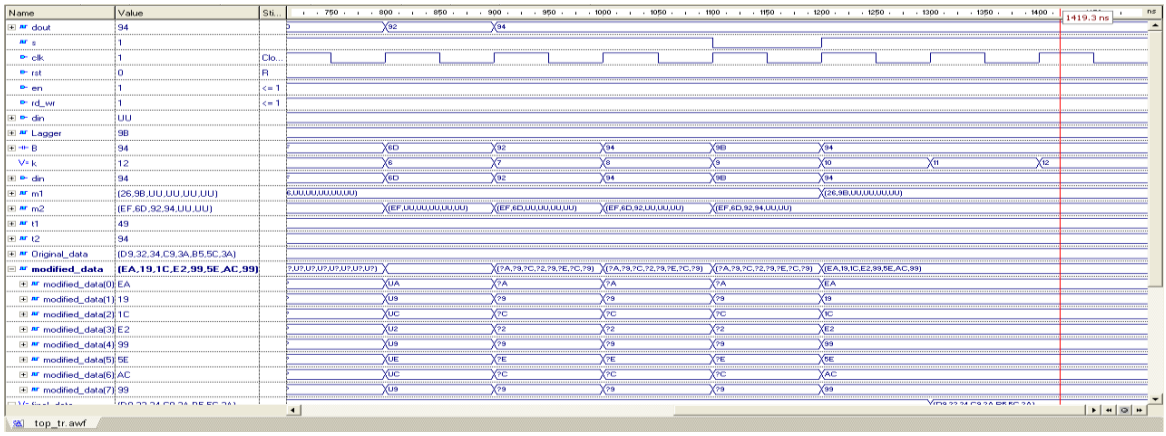


Figure 8 figure illustrating the bus , Sequencing and input data line for the designed encoder and decoder unit

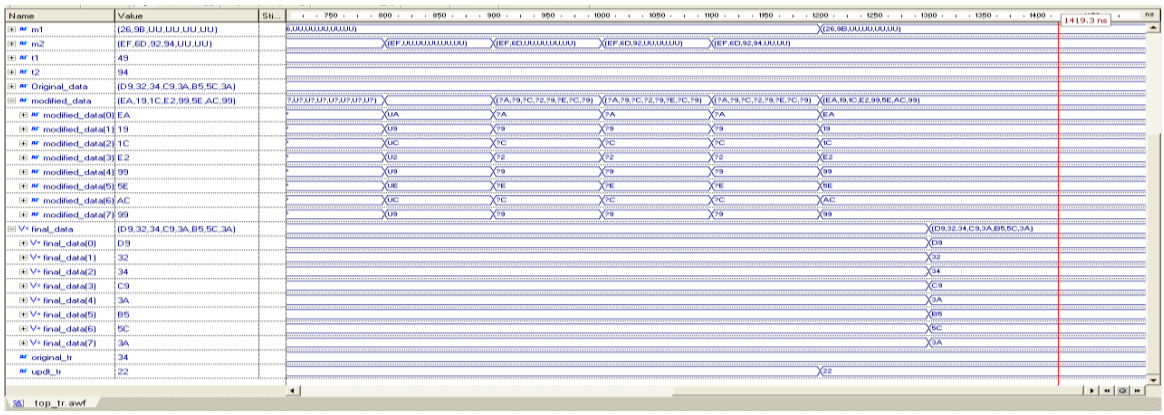


Figure 9. Illustrating the content of the BIST buffered data for regeneration and the reconstructed data from it.

The implementation of the proposed work onto the Xilinx device is carried out, the observed implementation summery is illustrated below.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	113	66,176	1%	
Number of 4 input LUTs	123	66,176	1%	
Logic Distribution				
Number of occupied Slices	134	33,088	1%	
Number of Slices containing only related logic	134	134	100%	
Number of Slices containing unrelated logic	0	134	0%	
Total Number of 4 input LUTs	261	66,176	1%	
Number used as logic	123			
Number used as a route-thru	138			
Number of bonded IOBs	34	992	3%	
IOB Flip Flops	14			
Number of PPC405s	0	2	0%	

Figure 10: Implementation summery of the synthesized proposed architecture

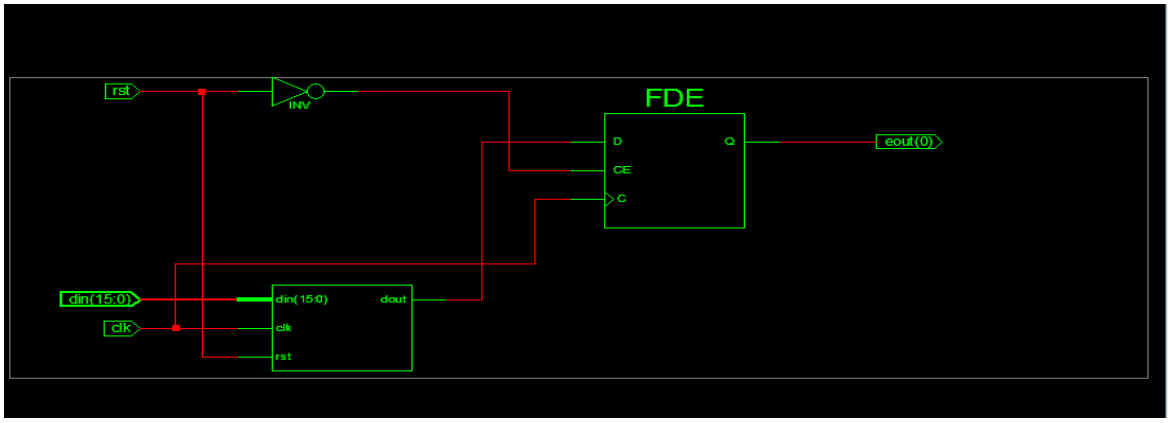


Figure 11: RTL visualization of the Implemented system

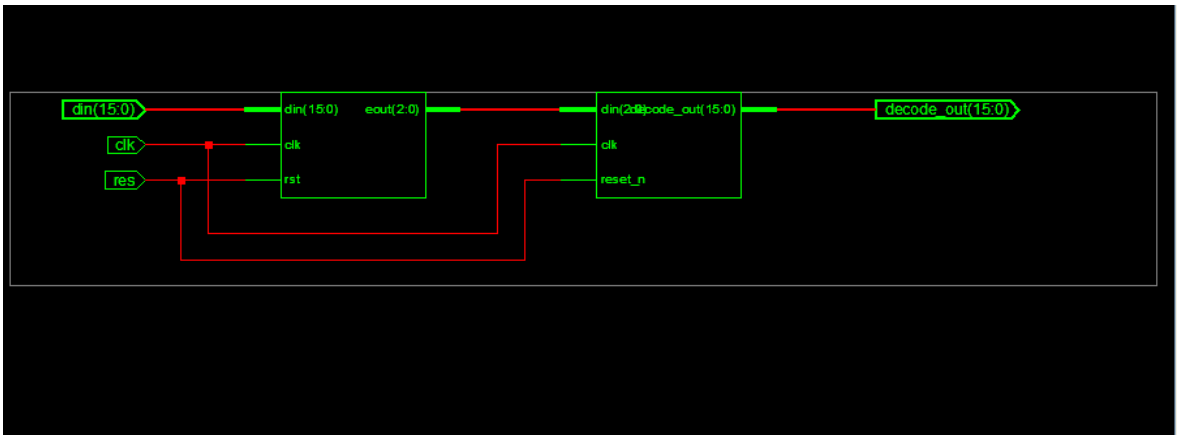
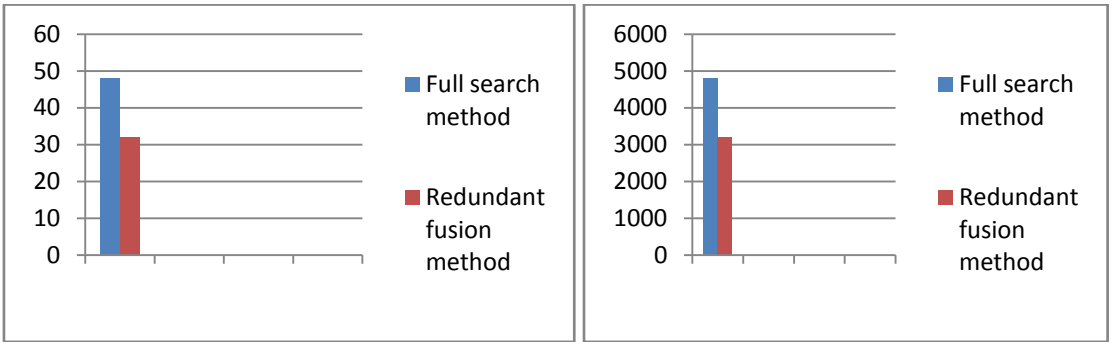


Figure 12: data flow in the Implemented design

A comparative analysis of this implementation is outlined in below tables. For a 2KB, (2048 x 16 bit)BIST unit, testing on 2 test patterns under a 100msec clock cycle.

a) Pattern Search Speed comparison



(a) (b)

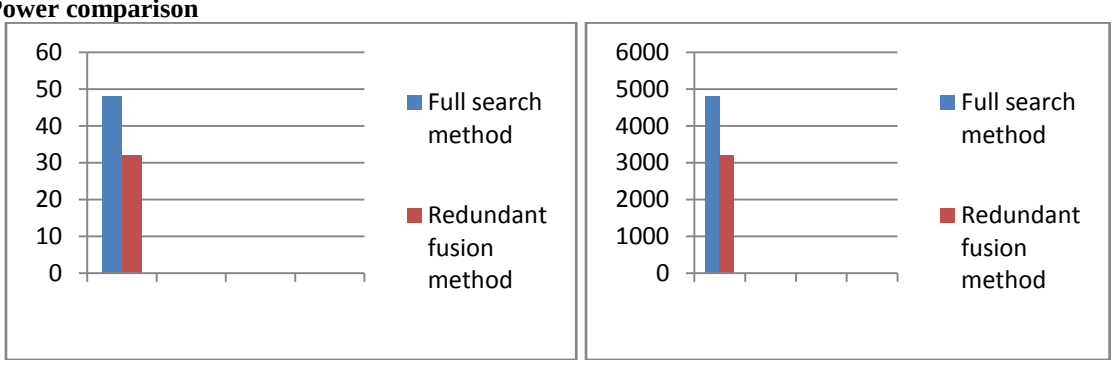
Figure 13: (a) Number of search clocks for pattern matching , (b) Time taken for search (mSec)

The observation for the method is outlined in the table below.

	No. of search clocks	Time taken (mSec)
Full search method	48	4800
Redundant fusion method	32	3200

Search speed is improved by 1600mSec ie. 16 clock cycles.

b) Power comparison



(a) (b)

Figure 14: (a) Number of search clocks for pattern matching , (b) Time taken for search

	No. of Transitions	Power consumed
Original pattern	28	183mW
Realign pattern	16	91mW

Power consumption is reduced by, 92mW

V. Conclusion

This paper outlined new interface architecture for DFT operation giving the advantage of higher speed of searching operation, Low power consumption in storage and processing. A high volume storage interface, with controlling in page BIST interface and a fault tolerant system for DFT interfacing, where the trained patterns are preserved for fault free condition. The DFT interface is given with the provisioning of self testing in both stuck 0 and stuck 1 operation and the pattern aligner unit save the transition hence minimizing the matching overhead and power consumption.

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